ASIM-X MEMS-Specific Design Rules

Version 2 – Revised April 5, 2006. This is a beta version, subject to change.
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1 Process Overview

ASIM-X, an acronym for "Application-Specific Integrated MEMS Exchange," is an implemention of a micromachining process flow to make bulk-silicon MEMS with electronics in foundry CMOS. This process flow and design rules were developed through the DARPA ASIMPS ("Application-Specific Integrated MEMS Process Service") project and the DARPA ASIM-X project at Carnegie Mellon University. The ASIM-X micromachining occurs after the CMOS is completed and is summarized with the series of cross sections in Figure 1. The structures are made from the silicon substrate, including the back-end-of-line CMOS metal-dielectric stack located on top of the substrate. The backside silicon deep reactive-ion etch step is setup to provide a silicon plate with a 50 μm ± 10 μm thickness on the frontside of the chip. The microstrutcures are then patterned from the frontside with a separate silicon DRIE step.

The metal layers in the CMOS process act as the etch mask for the frontside structural dielectric etch. The first metal layer to be encountered by the dielectric etch will mask the etch. The structural height is primarily determined by the silicon plate thickness. However, the appropriate metal and dielectric stack height must be added to the silicon height to determine the total height. Therefore, a discrete set of structure heights are available by specifying a particular metal etch-stop layer for the dielectric etch. For example, for a 4-metal CMOS process, four different structural heights may be specified. Gate polysilicon and any other CMOS layers that are placed under metal (including active device layers) are incorporated into the structure.

For the initial beta prototype run, the CMOS process will be restricted to one of the following processes:

- Jazz Semiconductor 4-metal 0.35 μm SiGe60 BiCMOS;
  die thickness is approximately 280 μm
- TSMC 4-metal 0.35 μm CMOS
- IBM 5HPE SiGe BiCMOS (4-metal 0.35 μm CMOS)

The beta users are responsible for purchasing the CMOS dice, most likely on a foundry multi-project run. Prior to tape-out, the submitted designs must pass the foundry design rules and the MEMS-specific design rules in this document.

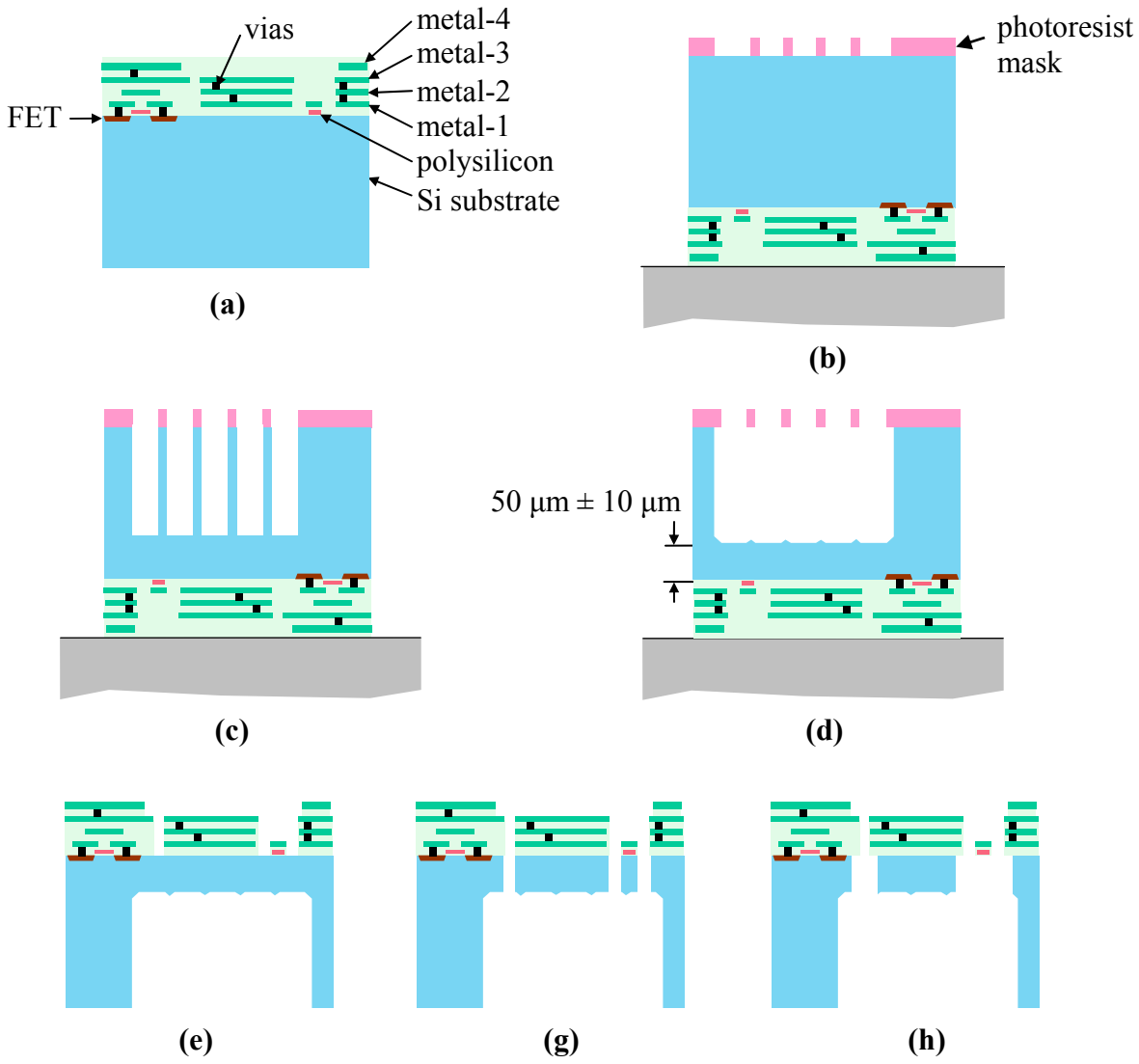


Figure 1. ASIM-X process flow. (a) Foundry CMOS before micromachining (4-metal CMOS shown); (b) Backside pattern with dry film photoresist; (c) Backside timed silicon DRIE; (d) Timed isotropic silicon etch; (e) RIE of dielectric stack down to the silicon substrate; (f) Frontside DRIE through silicon plate; and (h) optional Si undercut of 1 µm each side.

2 Layer and Pad Definitions

The CMOS layers of interest for MEMS design are:

POLY	:= gate polysilicon
METAL*n*	:= *n*'th level interconnect metallization; *n* = 1, 2, 3 or 4
VIA*ij*	:= via between metal layer *i* and metal layer *j*
CONTACT	:= via between METAL1 and either POLY or silicon diffusion implant regions
ACTIVE	:= active region (no field oxide)
RES_PROT	:= implant and/or silicide blocking layer (for high resistance polysilicon resistors)
NITRIDE	:= opening in silicon nitride passivation for pad access

The CMOS mask layers are used to construct several derived layers:

TRANSISTOR	:= ACTIVE & POLY
DIFF_CONT	:= CONTACT & ACTIVE & (NOT POLY)
POLY_RES	:= POLY & RES_PROT
STRUCTURE	:= METAL1 | METAL2 | METAL3 | METAL4"
STRUCT_BLOAT	:= METAL1 | METAL2 | METAL3 | (Bloat METAL4 by 0.5 μm)
SI_PLATE	:= Si plate area, inside of the 450 μm perimeter of the chip layout
SI_STRUCT	:= Bloat (Shrink STRUCT_BLOAT by 5 μm) by 5 μm
THIN_STRUCT	:= STRUCT_BLOAT with width < 3 μm
OTHER_STRUCT	:= STRUCT_BLOAT & (NOT SI_STRUCT) & (NOT THIN_STRUCT)
SPACE	:= NOT STRUCTURE
EFFECTIVE_SPACE	:= NOT STRUCT_BLOAT
EFFECTIVE_SI_SPACE	:= EFFECTIVE_SPACE with width > 3 μm
BONDPAD	:= designates a special bondpad cell (see discussion below)
OTHERPAD	:= NITRIDE & (NOT BONDPAD)

The derived layers are not used in CMOS chip production and are not recognized by the CMOS foundry. They exist solely for design rule check of the context-dependent rules in the MEMS areas. In the design rule checks for SPACE rules, the top METAL4 layer is bloated to reflect the greater difficulty in etch release of very high-aspect ratio structures.

In the DRC implementation in Cadence, a set of switches in the DRC dialog box are available and are detailed in Section 7. Each section below is checking for a specific type of rule, and has an associated DRC switch that needs to be set to activate checking of that rule. To check all the rules, set the *ALL* switch.

SI_PLATE, SI_STRUCT, THIN_STRUCT and OTHER_STRUCT

Several derived layers are available to identify various structural regions. SI_PLATE is the region of the chip where the silicon is thinned to 50 μm. SI_STRUCT is a derived layer to indicate strutcural regions where some amount of silicon plate area is connected to the structure. THIN_STRUCT indicates structures where all silicon is undercut. OTHER_STRUCT indictaes other structural regions that may have some silicon underneath, or may be completely undercut with silicon.

BONDPAD and OTHERPAD

Pads meant for wirebonding are recommended to be at least 200 μm by 200 μm in size to enable robust wirebonding. Overglass removal precludes use of smaller bondpads since off-center wire bonds may short to the metal covering the field. A cell called "bondpad" is provided with a fixed 86 μm by 86 μm nitride opening (defined by the NITRIDE drawing layer) and surrounding STRUCTURE out to 200 μm (that implements the metal bondpad plus the electrical isolation to the rest of the field). The DRC defines "BONDPAD" as the total 200 μm by 200 μm area and keys off the 86 μm by 86 μm nitride opening to identify a BONDPAD. A frontside BONDPAD frame layout in Figure 2 is recommended for most designs.

Pads for other uses, such as wafer probing and RF probing are allowed. These must be defiined by nitride openings other than 86 μm by 86 μm and the nitride opening is defined during DRC as "OTHERPAD". Note that the BONDPAD definition includes surrounding STRUCTURE, while the OTHERPAD definition does not include any STRUCTURE enclosure.

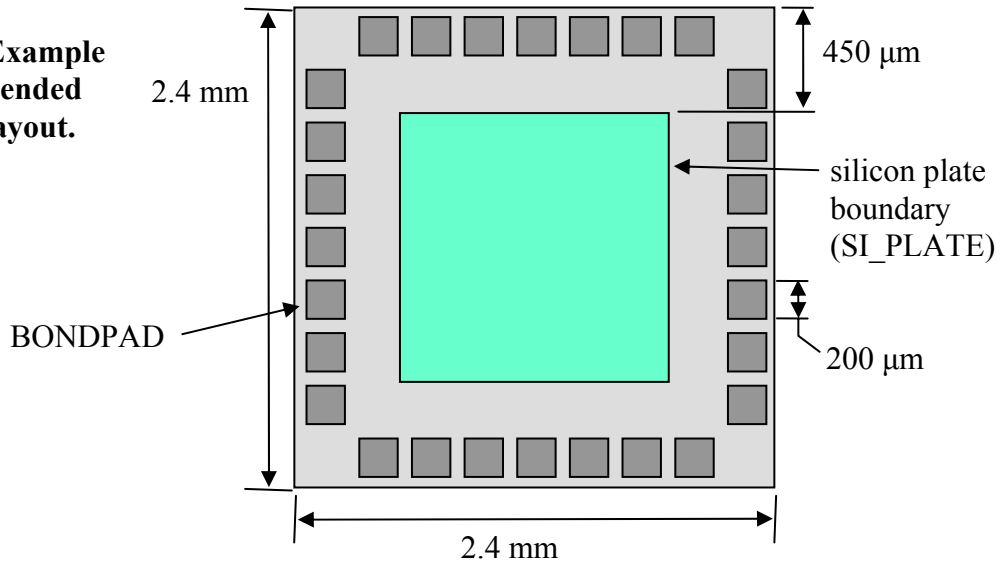


Figure 2. Example of recommended bondpad layout.

3 General Requirements

1.1 Grid Size — see vendor requirements

1.2 Corners — see vendor requirements

As these values are set by the foundry CMOS manufacturer, there is no switch in the rules file to check these rules. Please use the design rule check file provided by the manufacturer. It is recommended to use a 0.1 μm or larger grid for most MEMS design to minimize small alignment errors during layout. Rules 1.3, 1.4, and 1.5 are checked when the *PERIPHERY* swicth is set.

1.3 Minimum chip width and length — 2.4 mm
The minimum chip size is necessary to ensure robust photolithography.

1.4 Frontside chip perimeter rule — 450 μm
The chip perimeter must be filled by a continguous "dummy" STRUCTURE region that extends a minimum of 450 μm from the chip edge. This rule prohibits released MEMS around the chip periphery and thus greatly reduces yield loss from chip handling. The backside mask defines the extent of the thinned silicon region, and therefore the area where bulk Si MEMS may be defined. This mask is fixed and is generated by Carnegie Mellon. The simplified mask is shown in Figure 3. The backside opening extends to 450 μm from the user-defined patterning along the edge of the chip. Please be aware that multi-project prototyping services often dice the physical chip larger than this user-defined chip edge.

1.5 Minimum spacing of BONDPAD to silicon plate boundary or chip edge — 50 μm
This rule ensures that BONDPADs are anchored and is checked (with Rule 1.6) when the *PAD* switch is set.

1.6 Minimum spacing of OTHERPAD to silicon plate boundary or chip edge — 50 μm
This rule ensures that OTHERPADs are anchored.

Rules 1.8 and 1.9 are checked when the *ELECTRONICS* switch is set.

1.7 Minimum STRUCTURE enclosure of TRANSISTOR — 10 μm

1.8 Minimum STRUCTURE enclosure of DIFF_CONT — 10 μm

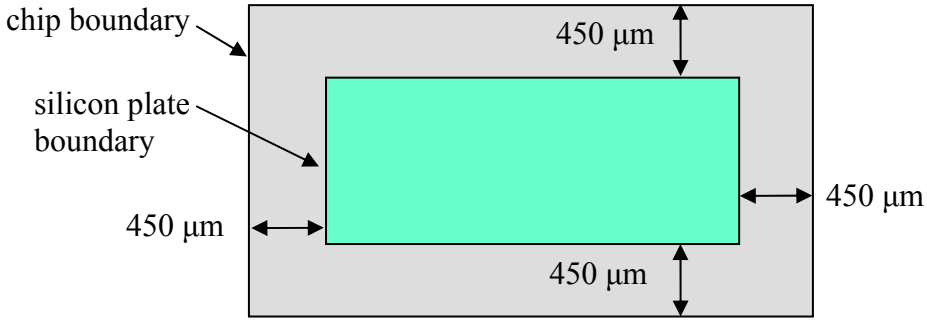


Figure 3. Simplified backside mask defining silicon plate.

4 SPACE Rules

Rules 2.1 through 2.5 define valid spacing around a STRUCTURE, and are checked when the *STRUCTSPACE* switch is set. The rules are defined in terms of *width*, which is the *smallest* layout dimension of the SPACE being checked, and *aspect ratio*, which is the ratio of length to width of the SPACE. METAL4 has different layout spacing limits due to the bloat of the layer creating two kinds of spacing limits: EFFECTIVE_SPACE and EFFECTIVE_SI_SPACE.

Rule 2.1 applies to EFFECTIVE_SPACE and EFFECTIVE_SI_SPACE, limiting the allowable maximum layout dimensions.

2.1 Maximum SPACE width 10 μm

The minimum EFFECTIVE_SPACE limits the possible gap between the top dielectric layers. Its value is dictated by the robustness of the frontside dielectric etch step. See Figure 4(a) for an example. This kind of gap may be useful for capacitive detectors or electrostatic actuators where a very narrow gap is desired. Corollaries of rule 2.2 are given in 2.2a-c to provide explicit effects for all combinations of STRUCTURE designed with and without METAL4.

2.2 Minimum EFFECTIVE_SPACE width 1.2 μm

- 2.2a Minimum SPACE between (STRUCTURE with no METAL4) to (STRUCTURE with no METAL4) edges 1.2 μm
- 2.2b Minimum SPACE between METAL4 to (STRUCTURE with no METAL4) edges 1.7 μm
- 2.2c Minimum SPACE between METAL4 to METAL4 edges 2.2 μm

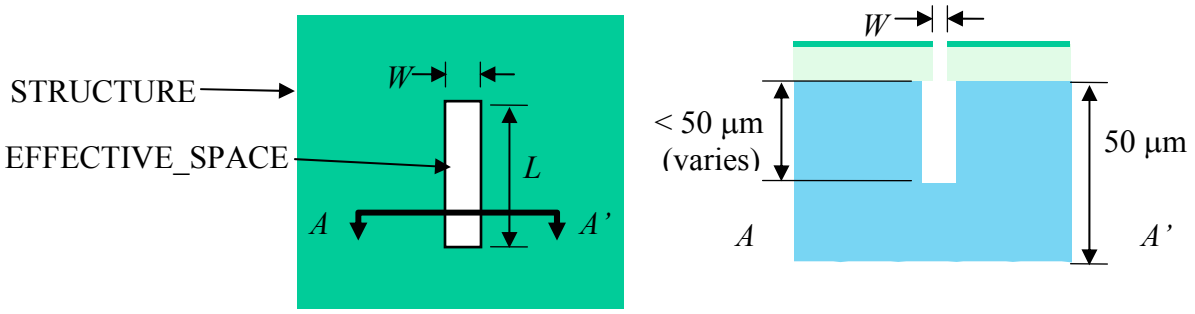
2.3 Minimum EFFECTIVE_SPACE aspect ratio for widths < 3 μm 5

The minimum EFFECTIVE_SI_SPACE limits the gap required to form structures out of the 50 μm-thick silicon plate. This value is set by the aspect-ratio-dependent etch limitation of the frontside deep reactive ion etch step. See Figure 4(b) for an example. Corollaries of rule 2.4 are given in 2.4a-c to provide explicit effects for all combinations of STRUCTURE designed with and without METAL4.

2.4 Minimum EFFECTIVE_SI_SPACE width 3.0 μm

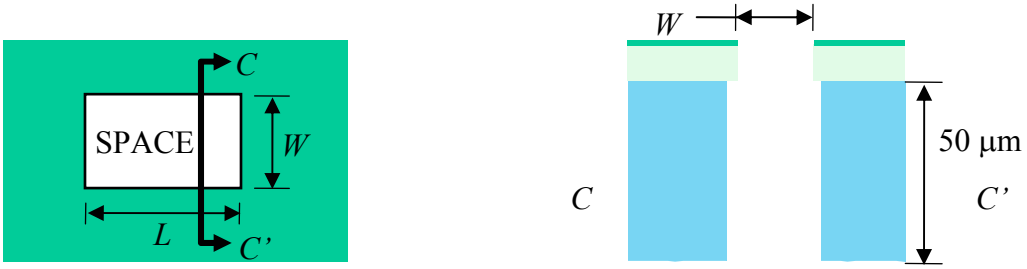
- 2.4d Minimum SPACE between (STRUCTURE with no METAL4) to (STRUCTURE with no METAL4) edges 3.0 μm
- 2.4e Minimum SPACE between METAL4 to (STRUCTURE with no METAL4) edges 3.5 μm
- 2.4f Minimum SPACE between METAL4 to METAL4 edges 4.0 μm

2.5 Minimum EFFECTIVE_SI_SPACE aspect ratio for widths < 5 μm 3



(a) Rule 2.2: 1.2 µm ≤ *W* < 3 µm, and Rule 2.3: *L*/*W* ≥ 5

(b) Rule 2.4: 3 µm ≤ *W* < 5 µm, and Rule 2.5: *L*/*W* ≥ 3



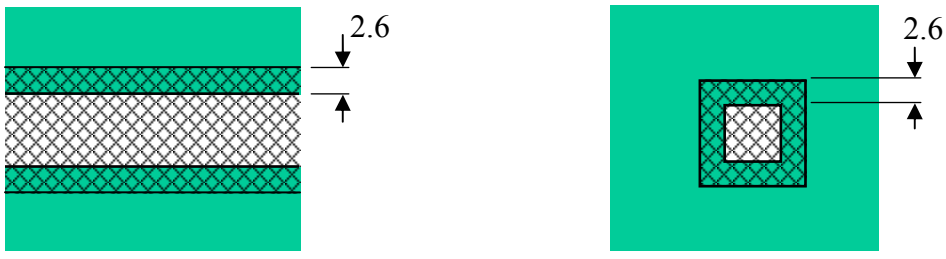
(c) *W* ≥ 5 µm, *L*/*W* ≥ 1

Figure 4. Examples of SPACE rules.

All SPACE regions need to be enclosed by ACTIVE. Rule 2.6 is checked when the *ACTIVE* switch is set. See Figure 5 for illustrations.

2.6 Minimum ACTIVE enclosure around SPACE 0.3 µm

Note that a diffusion region must be placed under ACTIVE to satisfy the CMOS vendor design rules. It is recommended that P+ diffusion be placed over ACTIVE for this purpose.



(a) **(b)**

Figure 5. Illustration of minimum ACTIVE enclosure for (a) a gap and (b) a hole. The cross-hatched regions are ACTIVE.

5 STRUCTURE Rules

The minimum silicon undercut of STRUCT_BLOAT adjacent to SPACE is 1 µm. This undercut distance provides a method for a thin-film dielectric structure that is 2 µm wide to be detached from the substrate, as indicated in Figure 6(a). Such an undercut is useful in forming thin springs or vertical metal-dielectric bimorphs from the CMOS interconnect stack.

The maximum silicon undercut of STRUCT_BLOAT adjacent to SPACE is 5.0 µm. A layout with STRUCT_BLOAT > 10 µm will ensure silicon is under the dielectric-metal stack, as shown in Figure 6(b).

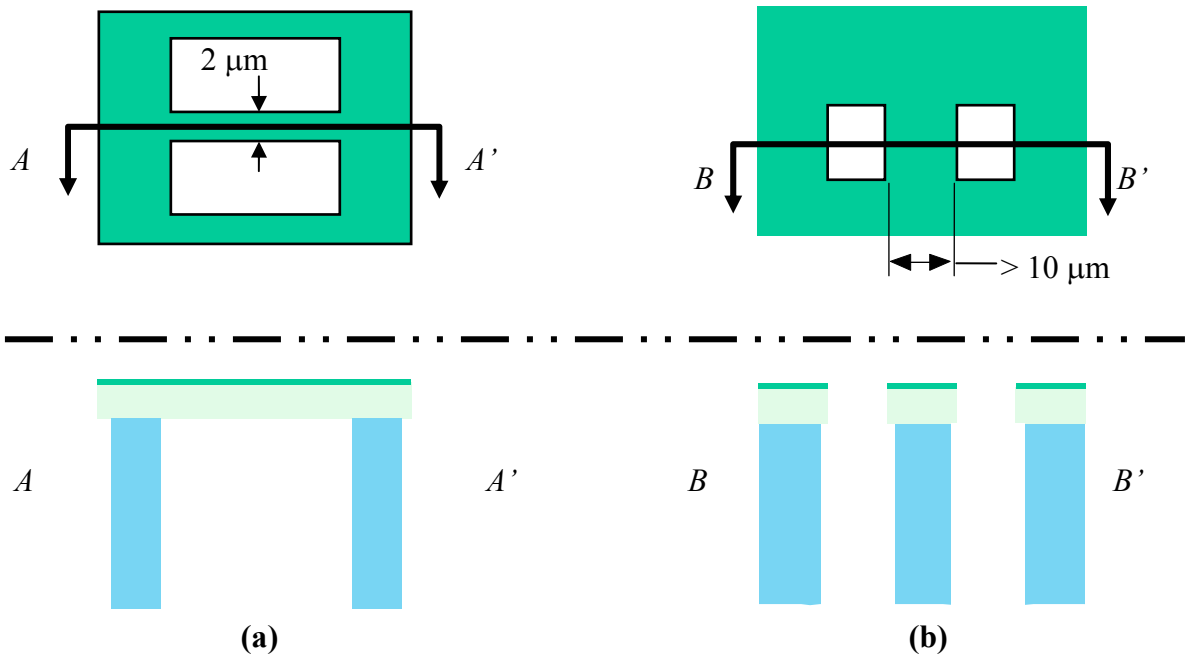


Figure 6. Illustration of (a) a 2 µm-wide STRUCTURE resulting in a suspended thin-film microstructure, and (b) a beam wider then 10 µm, resulting in a STRUCTURE with silicon connected underneath.

Rule 3.1 defines minimum valid STRUCTURE width, and is enabled when the *STRUCTWIDTH* switch is set.

3.1 Minimum STRUCTURE width 1.0 µm

Rules 3.2 and 3.3 define contact integrity in suspended structures, and are checked when the *VIA* switch is set. See Figure 7(a) and (b) for ilustrations.

3.2 Minimum VIAn enclosure by METAL*n*+1 0.6 µm

Rules 3.3 and 3.4 ensure that polysilicon inside of a structure remains intact after the post-CMOS micromachining steps, and are checked when the *POLY* switch is set. Rule 3.3 states that polysilcion must be enclosed in a structure so that the silicon release etch does not attack the polysilicon. Rule 3.4 enforces polysilicon in a structure to have field oxide underneath. Without field oxide, there is a reliability issue with the silicon release etch penetrating the thin gate oxide

layer and etching the polysilicon. Rule 3.4 applies only to areas within 10 µm of a SPACE.

3.3 Minimum POLY enclosure by METAL*n* 0.6 µm

3.4 Minimum POLY to ACTIVE spacing (within 10 µm from SPACE) 0.3 µm

Rule 3.5 guarantees structural continuity of a suspended structure in the presence of manufacturing offsets between metal layers. The rule is checked when the *OVERLAP* switch is set. See Figure 7(c) for an ilustration.

3.5 Minimum METAL*n* overlap by (STRUCTURE without METAL*n*) 0.3 µm

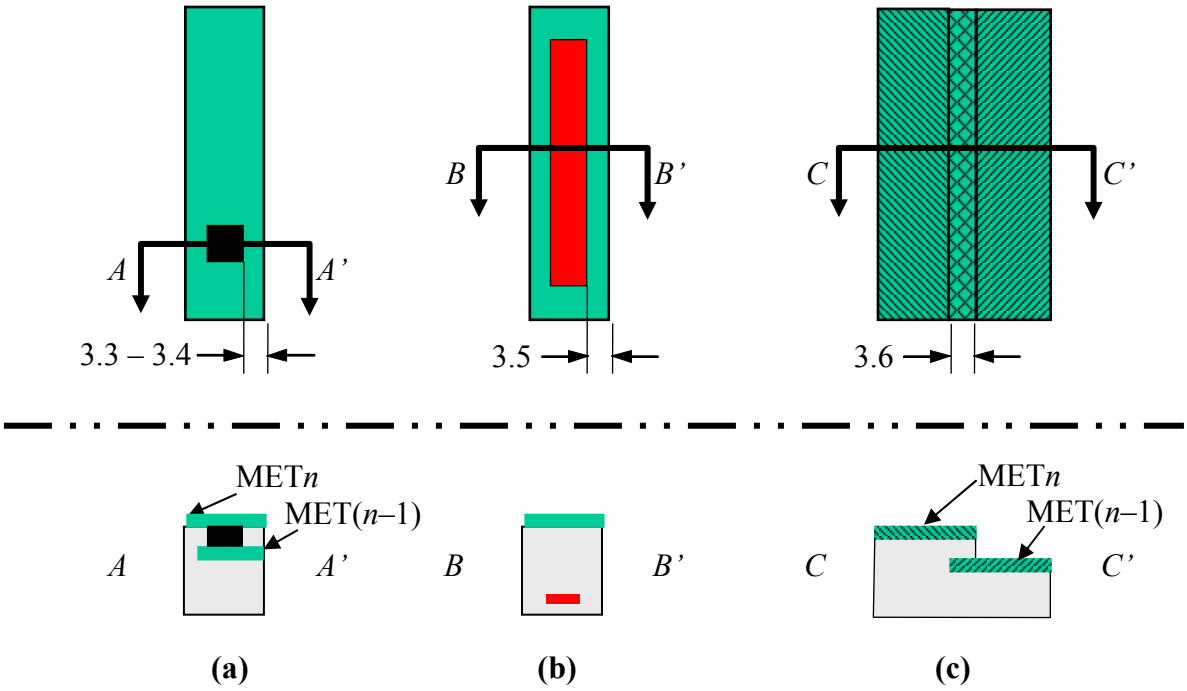


Figure 7. Structural enclosure and overlap rules. (a) Minimum contact/via enclosure; (b) Minimum polysilicon enclosure and (c) Minimum MET*n* overlap by (STRUCTURE without MET*n*). The cross-hatching is to distinguish the metal *n* and *n* – 1 layers.

6 Floating Metal

Rules 4.1 and 4.2 ensure that no metal is left electrically floating. The presence of floating metal can lead to anomolous drift in capacitive sensors and electrostatic actuators due to charging and charge leakage. Rule 4.1 is default with the *RES* switch off. Rule 4.2 is an alternative rule enabled with the *RES* switch on. This rule relaxes the floating metal DRC to allow METAL*n* connected to POLY enclosed by the RES_PROT layer (lightly doped drain implant blocking).

4.1 All METAL*n* must be contacted to BONDPAD, OTHERPAD or DIFF_ACT.

4.2 All METAL*n* must be contacted to BONDPAD, OTHERPAD, DIFF_ACT or POLY_RES.

7 DRC Switch Options

The MEMS Design Rule Checker (DRC) in Assura generates STRUCTURE and SPACE layers to aid visual debugging. These layers are available for viewing by selecting in the Assura VLW window.

The MEMS design rule check in Assura has several switches to turn on or off certain rules:

ALL	Check for all MEMS DRC.
PERIPHERY	Only checks Rules 1.3, 1.4 and 1.5
PAD	Only checks Rules 1.6 and 1.7 (also generates BONDPAD and OTHERPAD for visual debugging)
ELECTRONICS	Only checks Rules 1.8 and 1.9
STRUCTSPACE	Only checks Rules 2.1 through 2.5
ACTIVE	Only checks Rule 2.6
STRUCTWIDTH	Only checks Rule 3.1
VIA	Only checks Rules 3.2 and 3.3
POLY	Only checks Rules 3.4 and 3.5
OVERLAP	Only checks Rule 3.6
FLOATING	Only checks for floating metal Rule 4.1 (see the *RES* switch)
RES	Must be used with *FLOATING*. Enables Rule 4.2 and turns off Rule 4.1.